

Dynamic Core Binding (DCB) approach for load balancing in parallelization with MPI/OpenMP

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Background

- One of the critical issues in achieving good parallel performance is load imbalance.
 - Load balance has to be kept at both thread and process levels with MPI/OpenMP parallelization.
- A Dynamic Core Binding (DCB) approach mitigates process-level load imbalance at the thread-level.**

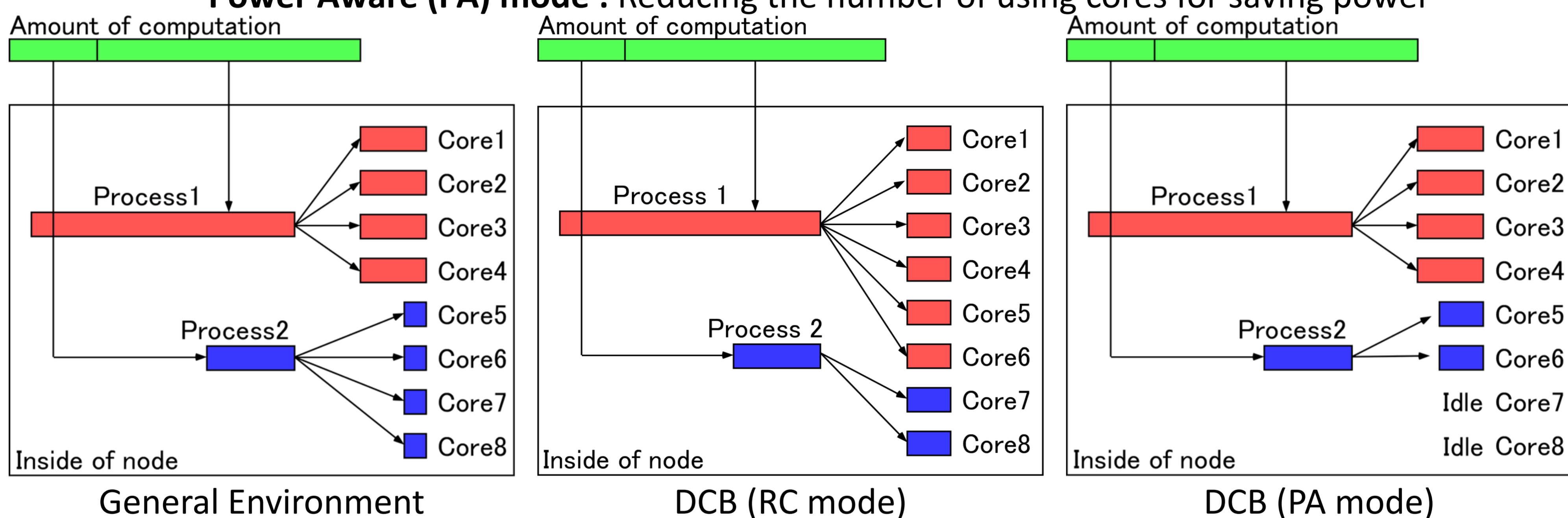
Dynamic Core Binding (DCB)*1

Idea of DCB : Changing the number of cores bound to each process based on loads of the processes

➔ **Load imbalance among the processes is balanced at the thread(core)-level.**

Preparing two modes based on different policies in the DCB approach

- **Reducing Computational-time (RC) mode** : Using all cores
- **Power Aware (PA) mode** : Reducing the number of using cores for saving power



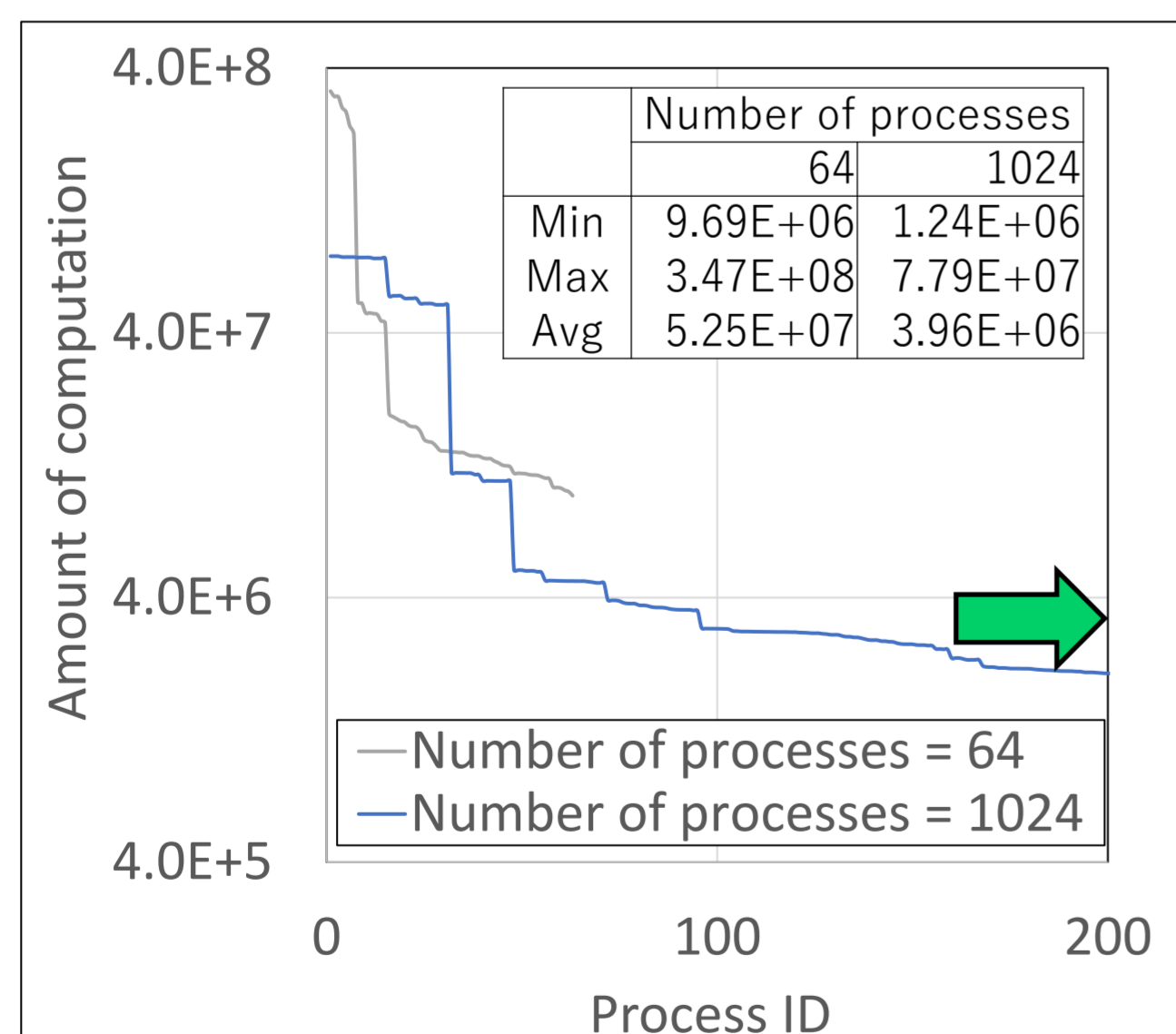
DCB only supports load balancing inside each node : we also consider load balancing among nodes.

➔ A hybrid approach combining RC and PA mode improve computational time and energy consumption at the same time*2.

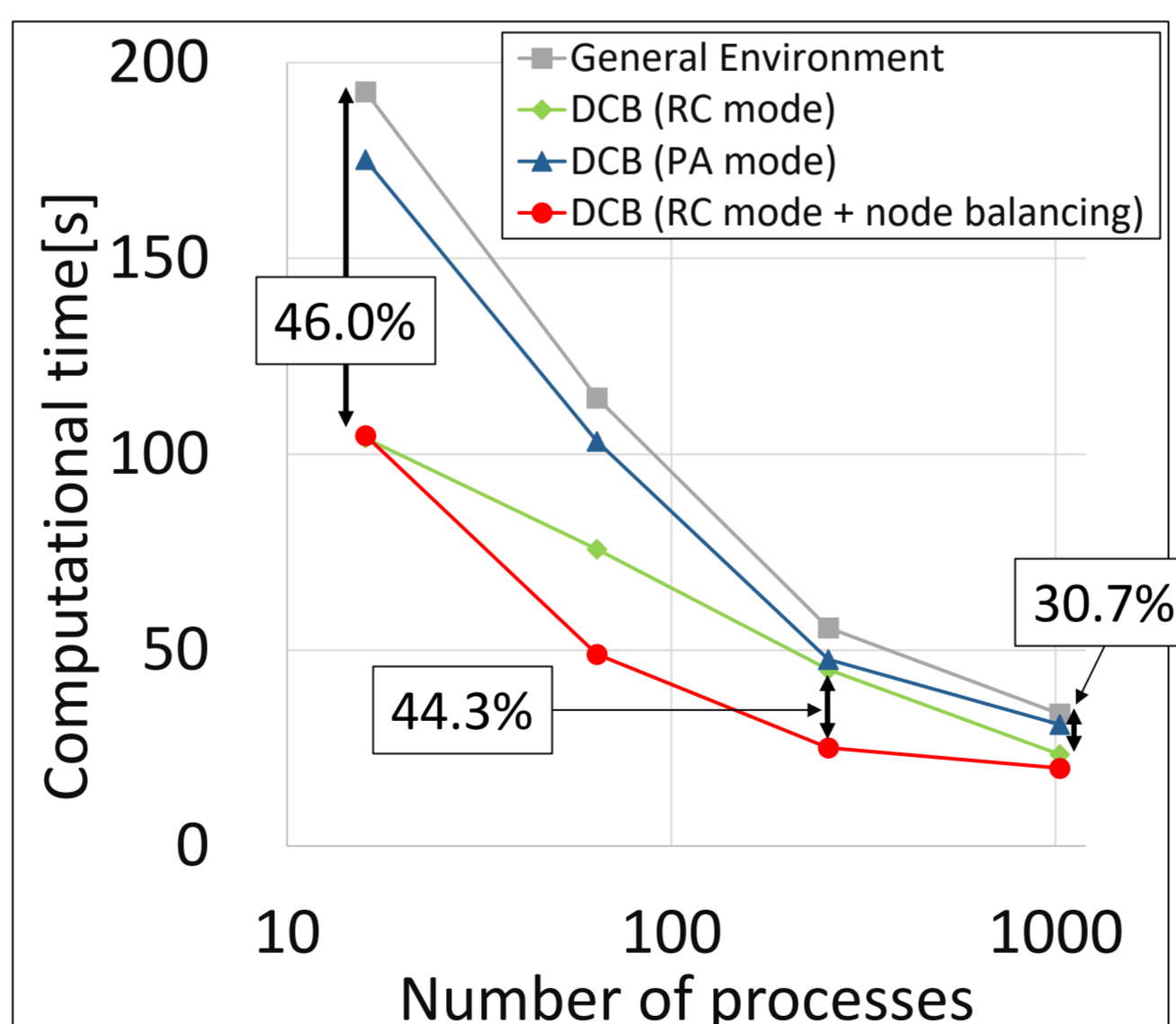
Result of numerical evaluations

Applying the DCB library to a lattice \mathcal{H} -matrix*3, which is optimized communication from the original. We use the Oakbridge-CX supercomputer for numerical evaluation.

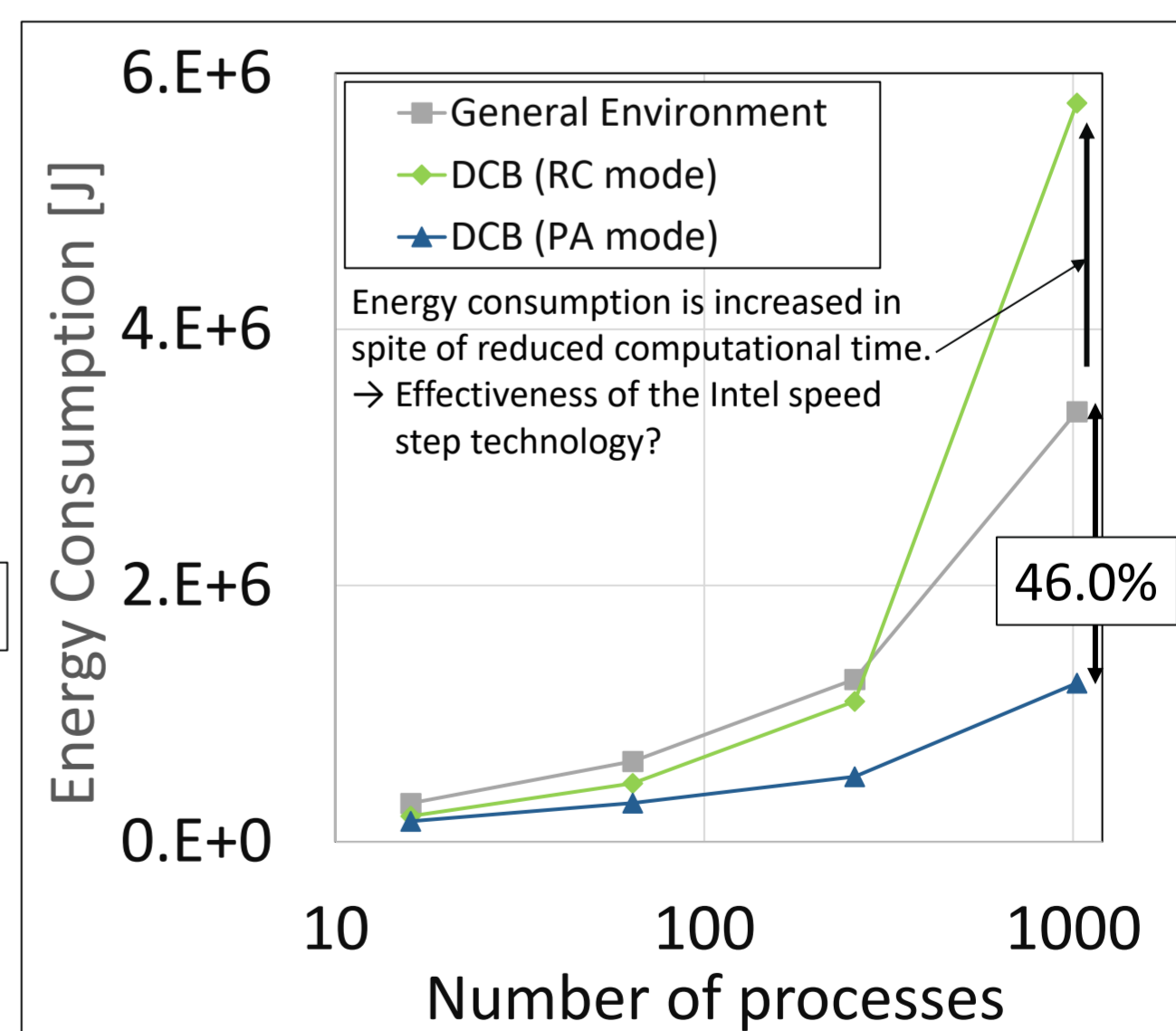
It evaluates the performance of 50 times multiplications of the lattice \mathcal{H} -matrix and vector .



Load imbalance among nodes



Effectiveness on computational time



Effectiveness on energy consumption

*1 M. Kawai, A. Ida, T. Hanawa and K. Nakajima, "Dynamic Core Binding for Load Balancing of Applications Parallelized with MPI/OpenMP.", International Conference on Computer Science(ICCS), 2023.

*2 M. Kawai, A. Ida, T. Hanawa, and T. Hoshino. "Optimize Efficiency of Utilizing Systems by Dynamic Core Binding", Workshop of International Conference on High Performance Computing in Asia-Pacific Region (HPC-Asia), 2024.

*3 A. Ida, "Lattice H-matrices on distributed-memory systems.", IEEE International Parallel and Distributed Processing Symposium (IPDPS), 2018.